



HUNT ENGINEERING
Chestnut Court, Burton Row,
Brent Knoll, Somerset, TA9 4BP, UK
Tel: (+44) (0)1278 760188,
Fax: (+44) (0)1278 760199,
Email: sales@hunteng.co.uk
<http://www.hunteng.co.uk>
<http://www.hunt-dsp.com>



For Sales and Support in North America Please Contact Our Strategic Partner:

Traquair Data Systems Inc, 114 Sheldon Road, Ithaca, NY 14850 USA

Tel 607 266 6000, Fax 607 266 8221

Email traquair@traquair.com, URL <http://www.traquair.com>

For Sales and Support in Other Areas Please Contact Your Local Reseller.

HUNT ENGINEERING

Dummy file

USER MANUAL

Hardware Rev A/C

Document Rev J

P. Warnes 22/8/02

COPYRIGHT

This documentation and the product it is supplied with are Copyright HUNT ENGINEERING 2001. All rights reserved. HUNT ENGINEERING maintains a policy of continual product development and hence reserves the right to change product specification without prior warning.

WARRANTIES LIABILITY and INDEMNITIES

HUNT ENGINEERING warrants the hardware to be free from defects in the material and workmanship for 12 months from the date of purchase. Product returned under the terms of the warranty must be returned carriage paid to the main offices of HUNT ENGINEERING situated at BRENT KNOLL Somerset UK, the product will be repaired or replaced at the discretion of HUNT ENGINEERING.

Exclusions - If HUNT ENGINEERING decides that there is any evidence of electrical or mechanical abuse to the hardware, then the customer shall have no recourse to HUNT ENGINEERING or its agents. In such circumstances HUNT ENGINEERING may at its discretion offer to repair the hardware and charge for that repair.

Limitations of Liability - HUNT ENGINEERING makes no warranty as to the fitness of the product for any particular purpose. In no event shall HUNT ENGINEERING'S liability related to the product exceed the purchase fee actually paid by you for the product. Neither HUNT ENGINEERING nor its suppliers shall in any event be liable for any indirect, consequential or financial damages caused by the delivery, use or performance of this product.

Because some states do not allow the exclusion or limitation of incidental or consequential damages or limitation on how long an implied warranty lasts, the above limitations may not apply to you.

TECHNICAL SUPPORT

Technical support for HUNT ENGINEERING products should first be obtained from the comprehensive Support section <http://www.hunteng.co.uk/support/index.htm> on the HUNT ENGINEERING web site. This includes FAQs, latest product, software and documentation updates etc. Or contact your local supplier - if you are unsure of details please refer to <http://www.hunteng.co.uk> for the list of current re-sellers.

HUNT ENGINEERING technical support can be contacted by emailing support@hunteng.demon.co.uk, calling the direct support telephone number +44 (0)1278 760775, or by calling the general number +44 (0)1278 760188 and choosing the technical support option.

TABLE OF CONTENTS

GETTING STARTED ON YOUR FPGA DESIGN ERROR! BOOKMARK NOT DEFINED.

WORKING THROUGH EXAMPLE 1.....	ERROR! BOOKMARK NOT DEFINED.
Preparing ISE	Error! Bookmark not defined.
Copying the examples from the HUNT ENGINEERING CD.....	Error! Bookmark not defined.
Opening the Example1 Project.....	Error! Bookmark not defined.
The Project's functional parameters.....	Error! Bookmark not defined.
Setting up the Configuration Package.....	Error! Bookmark not defined.
User Timing Constraints.....	Error! Bookmark not defined.
Creating the Bitstream for Example1	Error! Bookmark not defined.
Simulating the complete design	Error! Bookmark not defined.

MAKING YOUR OWN FPGA DESIGN..... 4

USER_AP INTERFACE	ERROR! BOOKMARK NOT DEFINED.
HARDWARE INTERFACE LAYER.....	ERROR! BOOKMARK NOT DEFINED.
IMPORTANT!.....	ERROR! BOOKMARK NOT DEFINED.
OTHER EXAMPLES.....	ERROR! BOOKMARK NOT DEFINED.
HOW TO MAKE A NEW DESIGN	ERROR! BOOKMARK NOT DEFINED.
Creating the Project	Error! Bookmark not defined.
Inserting your own Logic.....	Error! Bookmark not defined.
Top-level fine tuning (using other special IO pins).	Error! Bookmark not defined.
User Timing Constraints.....	Error! Bookmark not defined.
HINTS FOR FPGA DESIGNS	ERROR! BOOKMARK NOT DEFINED.
Use of Clocks.....	Error! Bookmark not defined.
Possible Sources of Clocks	Error! Bookmark not defined.
Flow Control.....	Error! Bookmark not defined.
Pipeline Length or “latency”	Error! Bookmark not defined.
I/O FROM THE FPGA.....	ERROR! BOOKMARK NOT DEFINED.
DSP WITH YOUR FPGA.....	ERROR! BOOKMARK NOT DEFINED.

Simulating the complete design

To generate the bitstream as above, you did not need to do any simulation. However, if you start modifying the provided examples and add your own code, verification will very soon become a central issue.

You will then need to install a VHDL simulator, like ModelSim (Xilinx Edition, Personal Edition, or Special Edition).

We provide behavioural simulation models for use at this stage. (`SIM_*.vhd` under `/common directory`, + test benches).

We will explain very briefly how to do a complete functional simulation of the design with ModelSim (any version except the demo version, a.k.a. "Starter" which is too crippled for that purpose).

ALSE has designed behavioural models for the FPGA's environment (FIFOs, HSB interface,...) that, coupled with the FPGA design, enable the user to simulate the complete application in a very realistic way. This simulation is usually purely functional, meaning that no timing is taken into account.

This is part of the Synchronous Design Methodology and makes sense when specific design rules have been respected, and when timing issues are verified by other means (like static timing analysis). Note that advanced users may perform timing simulations (post-layout, Vital).

1. Start ModelSim.
2. Change the current directory to Example1/Sim :
`cd x:/xxx...xxx/Example1/SIM` (replace the X's with your path)
3. Verify that the Xilinx-specific primitives libraries `UNISIM` and `XilinxCoreLib` are properly set up and accessible. you may use the "Design > Browse library" command for that purpose.
If these libraries are not properly compiled and/or mapped, you will not be able to simulate the design. In this case, refer to the Xilinx documentation (the steps to follow differ with the ModelSim versions). Just a hint : do *NOT* recompile the libraries if you are using the XE version...
4. From the transcript window, type :
`do simu.do`
or use the GUI command "Macro > Execute Macro" and select `simu.do`.

ModelSim should then compile all the design units, load the test bench, display all the top-level signals in the Waveform viewer, run the simulation, issue messages in the transcript, and stop the simulator. Note that vector Files are read and created during the simulation.

The simulation has created `Fifo_out.txt` that you may compare with `Fifo_In.txt` !

You may use the DOS command:

```
fc Fifo_In.txt Fifo_out.txt.
```

This should prove that the data flows correctly :

Input file → External Fifo_In model → FPGA's Fifo interface

- User_Ap1's Internal control logic → FPGA's Fifo out Interface
- External Fifo_Out model → Output file.

You could now investigate and see how we have built the simulation environment, and specifically the behavioural models (which read and write from/to text files).

If you look at the waveforms, you will notice that our External Fifo behavioural models do simulate some irregular data flow (with busy times) to ensure that the Full/Empty logic works fine.

Contact ALSE if you are interested in specific models and/or training courses.